Abstracts

Modeling and Simulation of Switching Noise Including Power/Ground Plane Resonance for High Speed GaAs FET Logic (FL) Circuits

J.-M. Jong and V.K. Tripathi. "Modeling and Simulation of Switching Noise Including Power/Ground Plane Resonance for High Speed GaAs FET Logic (FL) Circuits." 1995 MTT-S International Microwave Symposium Digest 95.3 (1995 Vol. III [MWSYM]): 1081-1084.

Equivalent circuit models of power/ground plane structures in high speed/frequency electronic packages used for switching noise and ground bounce simulation are presented. As an example, the effect of package resonance on the switching noise due to edge and clock rates of the GaAs FET logic (FL) inverter is reported for a typical MLC package.

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